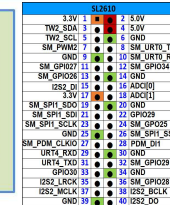


Block Diagram



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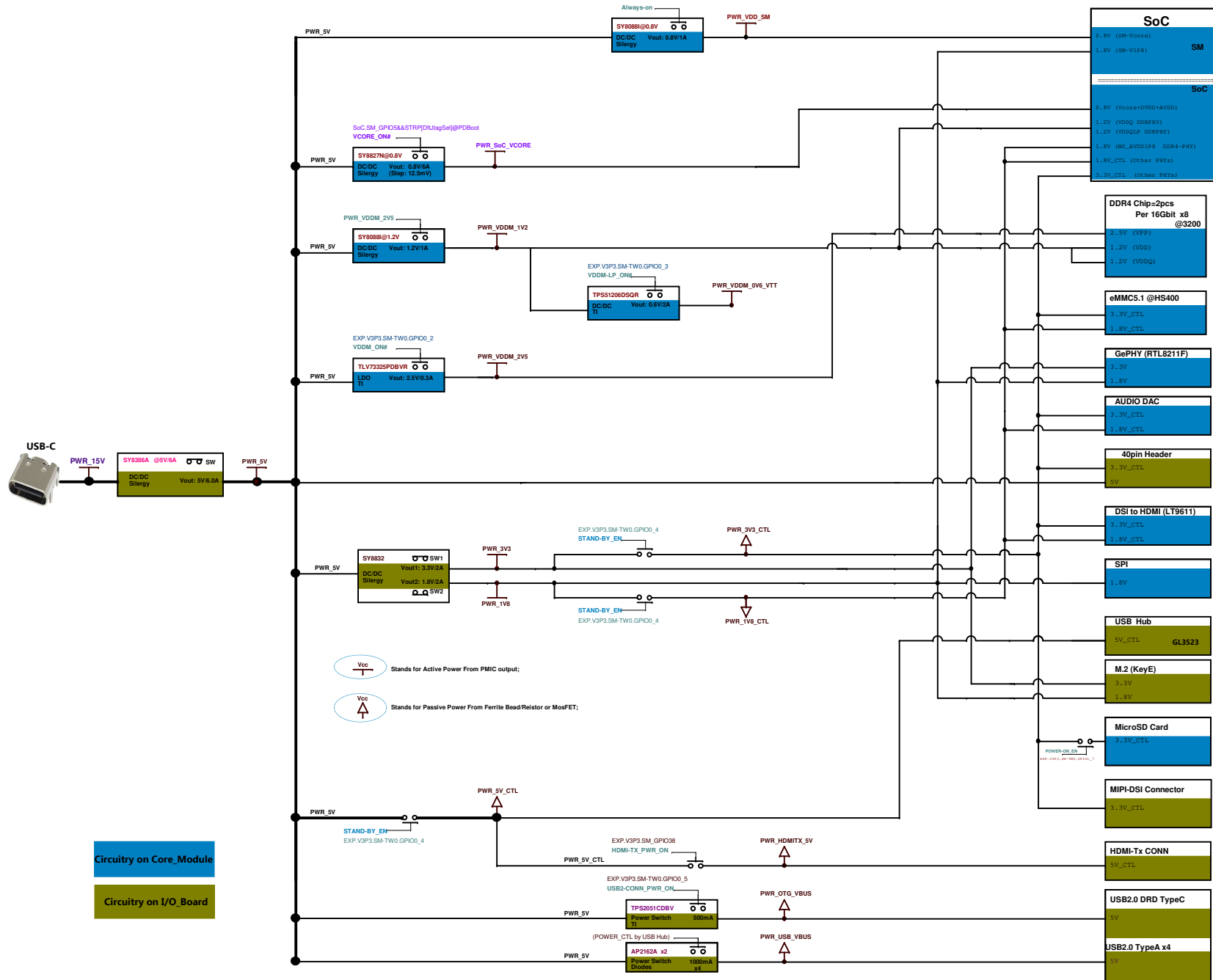
01: TITLE & BLOCK DIAGRM
02: REVISION HISTORY
03: POWER TREE
04: SL2610 - SM MISC
05: SL2610 - SOC MISC
06: SL1620 - DDR4_PHY
07: SL2610 - MIPI-CSI, MIPI-DSI
08: SL2610 - SDIO1, USB, eMMC
09: SL2610 - PWR/GND
10: SL2610 - STRAP
11: MEM - DEV DDR4
12: MEM - eMMC, SPI
13: PERIF - ETH_RTL8211F
14: PERIF - DSI_HDMI Converter
15: CONN - AUDIO DAC/DMIC
16: CONN - RGMII1
17: CONN - SD CARD
18: PWR - VDDM_2V5/1V2/VTT
19: PWR - VCORE/SM_VDD
20: Current-Measurement
21: SODIMM - GoldFinger

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REVISION HISTORY

Rev#	Date	Originator (s)	Rev Item ID	What Revised	Why Revised	SW Impacts	Other Impacts	Rework# Base On Previous Version	SW Version SS[3:0]
A	04/10/2025	William W	1	SCH for SL2610 Core-Module	SL2610-RDK design	NO	NO		0001
B	10/11/2025	William W	1	Change R217 from 10K to 33K.	Optimize system power up sequence.	NO	NO	Rework-A	0000
			2	Add R274 2.2K pull-down resistor to STRP[pIIBypass]	Optimize design	NO	NO	Rework-B	
			3	Change L20 to 0R resistor.	Improve SDR50 performance	NO	NO	Rework-E	
			4	Change Pin-Demux for both SM_URT0 and SM_URT1 and rename net alias	Optimize design	Yes	NO		
			5	Update SOC symbol and add R276	Optimize design	NO	NO		
			6	Change R34 from DNS to 2.2K	SS[3:0] changes from 4'b0001 to 4'b0000	Yes	NO		
C	11/28/2025	William W	1	Change R39=2.2K, R43=20K, R44=1K.	Improve compatibility for external Uart debug board	NO	NO	Rework-A	0010
			2	Add text for software_strap[0][1]	Distinguish board version and DDR size	Yes	NO		
			3	Update Blockdiagram with DDR4@2GB as default and update U2,U3,R35	Update DDR4@2GB as default	Yes	NO		
D	01/18/2026	William W	1	Remove C233, change C230=0.01uF	Optimize SD power up sequence	NO	NO		0010
			2	Change Parts to PGB2010402KRHF from AVR-M1005C270MTABB	Meet Halogen-Free	NO	NO		
			3	Change Block Diagram and DDR4 part with selectable memory size.	Selectable memory size	NO	NO		

Power Tree



MISC	
SM_XTAL_I	G31
SM_XTAL_O	F31
SM_XTAL32K_I	E30
SM_XTAL32K_O	F30
SM_RSTn	U29
SM_POR_EN	V31
SM_TRSTn	W26
SM_TCK	W30
SM_AUDIO_MUTE	T29
CAMERA_MUTE	W25
SM_ADCIO	B26
SM_ADCI1	B27
SM_ADCI2	A26
SM_ADCI3	B28
SM_ADCI4	B29
SM_ADCI5	B30
SM_ADCI6	C30
SM_ADCI7	D30

SL2610 - 12x13

U1D

OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	BootStrap	SM_GPIO
SM_TMS	SM_GPIO0	SM_URTO_TXD	KEY_COL0	GPIO_TRIG0	SM_PDM_DIO	SM_PWM10		PBBoot	SM_GPIO0
SM_TDI	SM_GPIO1	SM_URTO_RXD	KEY_COL1		SM_PWM9	KEY_ROW7		PBBoot	SM_GPIO1
SM_TDO	SM_GPIO2	SM_PDM_CLKIO	1252_MCLK			SM_PWM11		PBBoot	SM_GPIO2
SM_GPIO3	SM_SPI1_SS0n	SM_TW1_SCL	SM_PWM6	SM_I3C_MS_SCL					SM_GPIO3
SM_GPIO4	SM_SPI1_SS1n	SM_TW1_SDA	SM_PWM0	SM_I3C_MS_SDA					SM_GPIO4
SM_GPIO5	SM_SPI1_SS2n		SM_PWM1					dft_jtag_sel	SM_GPIO5
SM_GPIO6	SM_SPI1_SS3n	SM_SPI15_SS0n	SM_PWM2						SM_GPIO6
SM_GPIO7	SM_URTO_RXD	SM_CANO_RX	KEY_ROW6	GPIO_TRIG2	SM_PWM9	SM_URTI_RXD		boot_src[0]	SM_GPIO7
SM_GPIO8	SM_URTO_TXD	SM_CANO_TX	SM_CLKOUT			SM_URTI_TXD		boot_src[1]	SM_GPIO8
SM_GPIO9	SM_SPI1_SDO	SM_SPI15_SDO	SM_PWM3						SM_GPIO9
SM_GPIO10	SM_SPI1_SCLK	SM_SPI15_SCLK	SM_PWM4						SM_GPIO10
SM_GPIO11	SM_SPI1_SDI	SM_SPI15_SDI	SM_PWM5						SM_GPIO11
SM_GPIO12	SM_TW0_SCL	SM_I3C_MS_SCL	SM_PWM6						SM_GPIO12
SM_GPIO13	SM_TW0_SDA	SM_I3C_MS_SDA	SM_CLKOUT						SM_GPIO13
SM_GPIO14	SM_TW1_SCL	SM_URTO_CTSn	SM_PWM10	SM_CANO_RX		SM_URTI_CTSn			SM_GPIO14
SM_GPIO15	SM_TW1_SDA	SM_URTO_RTSn	SM_PWM11	SM_CANO_TX		SM_URTI_RTSn			SM_GPIO15
SM_GPIO16	SM_URTI_RXD	SM_CANO_RX	SM_PWM7					pll_bypass	SM_GPIO16
SM_GPIO17	SM_URTI_TXD	SM_CANO_TX	SM_PWM8			SM_URTO_TXD			SM_GPIO17
SM_GPIO18	SM_XSPI_CS0n								SM_GPIO18
SM_GPIO19	SM_XSPI_DATA0								SM_GPIO19
SM_GPIO20	SM_XSPI_DATA1								SM_GPIO20
SM_GPIO21	SM_XSPI_DATA2								SM_GPIO21
SM_GPIO22	SM_XSPI_DATA3								SM_GPIO22
SM_GPIO23	SM_XSPI_CLK								SM_GPIO23
SM_GPIO24	SM_XSPI_CLKn								SM_GPIO24
SM_GPIO25	SM_XSPI_DQS								SM_GPIO25
SM_GPIO26	SM_XSPI_CS1n	SM_URTI_TXD	KEY_COL2	SM_URTI3_RTSn	SM_URTI3_DE	KEY_ROW6	SM_CLKOUT		SM_GPIO26
SM_GPIO27	SM_XSPI_DATA4	SM_URTI2_RXD	KEY_COL3	SM_URTI3_CTSn	SM_URTI3_Rsn	KEY_ROW4			SM_GPIO27
SM_GPIO28	SM_XSPI_DATA5	SM_URTI3_TXD	KEY_COL4	SM_URTI2_RTSn	SM_URTI2_CTSn	KEY_ROW3			SM_GPIO28
SM_GPIO29	SM_XSPI_DATA6	SM_URTI3_RXD	KEY_COL5	SM_URTI2_CTSn	SM_URTI2_Rsn	KEY_ROW2			SM_GPIO29
SM_GPIO30	SM_XSPI_DATA7		KEY_COL6						SM_GPIO30
SM_GPIO31	SM_PWM0	SM_URTI_RXD	KEY_ROW7	SM_PDM_DIO	SM_URTO_RXD	SM_CANO_RX			SM_GPIO31
SM_GPIO32	SM_PWM1	SM_URTI_TXD	KEY_ROW8	SM_PDM_CLKIO	SM_URTO_TXD	SM_CANO_TX			SM_GPIO32
SM_GPIO33	SM_PWM2	SM_URTI2_TXD	SM_URTI3_RTSn	SM_URTI3_DE	SM_URTI3_Rsn				SM_GPIO33
SM_GPIO34	SM_PWM3	SM_URTI2_RXD	SM_URTI3_CTSn	KEY_ROW4	SM_URTI3_Rsn				SM_GPIO34
SM_GPIO35	SM_PWM4	SM_URTI1_RTSn	SM_URTI2_CTSn	KEY_ROW3	SM_URTO_RTSn				SM_GPIO35
SM_GPIO36	SM_PWM5	SM_URTI1_CTSn	SM_URTI3_RXD	SM_URTI2_CTSn	SM_URTO_CTSn				SM_GPIO36
SM_GPIO37	SM_PWM6		SM_TW0_SCL	KEY_ROW6	SM_PDM_CLKIO				SM_GPIO37
SM_GPIO38	SM_PWM7		SM_TW0_SDA		SM_PDM_DIO				SM_GPIO38

SL2610 - 12x13

V30	SoC.SM.TMS&SM.GPIO0	>>>SoC.SM.TMS&SM.GPIO0 [13,16,21]
T30	SoC.SM.TDI&SM.GPIO1	>>>SoC.SM.TDI&SM.GPIO1 [21]
U30	SoC.SM.TDO@I2S2.MCLK	>>>SoC.SM.TDO@I2S2.MCLK [21]
C24	SoC.SM.TW1.SCL	>>>SoC.SM.TW1.SCL [19,21]
A24	SoC.SM.TW1.SDA	>>>SoC.SM.TW1.SDA [19,21]
B24	SoC.SM.GPIO5&STRP[DIUtagSel]@PDBoot	>>>SoC.SM.GPIO5&STRP[DIUtagSel]@PDBoot [10,19]
B25	SoC.SM.SPI1.SS3n	>>>SoC.SM.SPI1.SS3n [21]
T31	SoC.SM.URTO.RXD	>>>SoC.SM.URTO.RXD [21]
U26	SoC.SM.URTO.TXD&STRP[boot_src0]@PUBoot	>>>SoC.SM.URTO.TXD&STRP[boot_src0]@PUBoot [10,21]
C23	SoC.SM.SPI1.SDO&STRP[boot_src1]@PDBoot	>>>SoC.SM.SPI1.SDO&STRP[boot_src1]@PDBoot [10,21]
P23	SoC.SM.SPI1.SDI	>>>SoC.SM.SPI1.SDI [21]
D24	SoC.SM.SPI1.SCLK	>>>SoC.SM.SPI1.SCLK [21]
U28	SoC.SM.TW0.SCL	>>>SoC.SM.TW0.SCL [20,21]
U25	SoC.SM.TW0.SDA	>>>SoC.SM.TW0.SDA [20,21]
P20	SoC.SM.URTI1.CTSn	>>>SoC.SM.URTI1.CTSn [21]
P30	SoC.SM.URTI1.RTSn	>>>SoC.SM.URTI1.RTSn [21]
R29	SoC.SM.URTI1.RXD	>>>SoC.SM.URTI1.RXD [21]
N30	SoC.SM.URTI1.TXD&STRP[pllBypass]@PDBoot	>>>SoC.SM.URTI1.TXD&STRP[pllBypass]@PDBoot [10,21]
P28	SoC.XSPI.CS0n	>>>SoC.XSPI.CS0n [12]
N31	SoC.XSPI.DATA0	>>>SoC.XSPI.DATA0 [12]
M30	SoC.XSPI.DATA1	>>>SoC.XSPI.DATA1 [12]
L31	SoC.XSPI.DATA2	>>>SoC.XSPI.DATA2 [12]
L30	SoC.XSPI.DATA3	>>>SoC.XSPI.DATA3 [12]
M27	SoC.XSPI.CLK	>>>SoC.XSPI.CLK [12]
M29	SoC.XSPI.CLK0	>>>SoC.XSPI.CLK0 [12]
P26	SoC.SM.GPIO25	>>>SoC.SM.GPIO25 [21]
L29	SoC.SM.GPIO26	>>>SoC.SM.GPIO26 [21]
K29	SoC.SM.GPIO27	>>>SoC.SM.GPIO27 [21]
J29	SoC.SM.GPIO28	>>>SoC.SM.GPIO28 [21]
H30	SoC.SM.GPIO29	>>>SoC.SM.GPIO29 [21]
H29	SoC.SM.CLKOUT	>>>SoC.SM.CLKOUT [21]
F19	SoC.SM.CAN1.RX&SM.PDM.DIO	>>>SoC.SM.CAN1.RX&SM.PDM.DIO [21]
A21	SoC.SM.CAN1.TX&SM.PDM.CLKIO	>>>SoC.SM.CAN1.TX&SM.PDM.CLKIO [21]
B21	SoC.SM.PWM2	>>>SoC.SM.PWM2 [21]
C21	SoC.SM.GPIO34	>>>SoC.SM.GPIO34 [21]
F21	SoC.SM.GPIO35	>>>SoC.SM.GPIO35 [13]
C22	SoC.SM.GPIO36	>>>SoC.SM.GPIO36 [14]
D22	SoC.SM.GPIO37	>>>SoC.SM.GPIO37 [15]
B22	SoC.SM.GPIO38	>>>SoC.SM.GPIO38 [14]

U1E

OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	BootStrap	GPIO
GPIO0	I2S1_LRCK						SPI3_SS0n		GPIO0
GPIO1	I2S1_BCLK						SPI3_SCLK		GPIO1
GPIO2	I2S1_DO			SPDIFO			SPI3_SDO		GPIO2
GPIO3	I2S1_MCLK			SPDIFI			SPI3_SS1n		GPIO3
GPIO4	I2S1_DI			SPDIFI			SPI3_SDI		GPIO4
GPIO5	I2S2_LRCK	CAM_FIXCLK	KEY_ROW0	SPDIFI		KEY_ROW7			GPIO5
GPIO6	I2S2_BCLK	CAM_HSNC	KEY_ROW1	SPDIFO		KEY_ROW6			GPIO6
GPIO7	I2S2_DO		KEY_ROW2	SPDIFO	SM_PDM_CLKIO	KEY_ROW5			GPIO7
GPIO8	I2S2_DI	CAM_VSYNC	KEY_ROW3	SPDIFI		KEY_COL4			GPIO8
GPIO9		CAM_DATA0		PDM_DI1					GPIO9
GPIO10		CAM_DATA1		PDM_DI2	DSI_TE				GPIO10
GPIO11	I2S2_MCLK	CAM_DATA7		SM_PDM_CLKIO					GPIO11
GPIO12	I2S3_LRCK	CAM_DATA3	SDIO2_WP	SDIO1_WP					GPIO12
GPIO13	I2S3_BCLK	PDM_DI1	RGMII_PTP_PPS_OUSB2_DRV_VBUS						GPIO13
GPIO14	I2S3_DO		PDM_DI3			SPDIFO			GPIO14
GPIO15	I2S3_DI	CAM_DATA4		SM_PDM_DI0		SPDIFI			GPIO15
GPIO16	SPI2_SS0n		SDIO2_DAT3						GPIO16
GPIO17	SPI2_SS1n	CAM_DATA5	SDIO2_DAT2		DSI_TE				GPIO17
GPIO18	SPI2_SS2n	CAM_DATA6	SDIO2_DAT1	PDM_DI2	SM_CAN1_RX				GPIO18
GPIO19	SPI2_SS3n	CAM_DATA7	SDIO2_DAT0	PDM_DI3	SM_CAN1_TX				GPIO19
GPIO20	SPI2_SDO		SDIO2_CMD						GPIO20
GPIO21	SPI2_SCLK		SDIO2_CLK		CLKOUT			software_strap[1]_PDBoot	GPIO21
GPIO22	SPI2_SDI		SDIO2_Cdn	SDIO1_Cdn					GPIO22
GPIO23	TW2_SCL	RGMII_MDC	KEY_ROW0		SPI3_SS2n	KEY_COL3			GPIO23
GPIO24	TW2_SDA	RGMII_MDIO	KEY_ROW1		SPI3_SS3n	KEY_COL2			GPIO24
GPIO25	URT5_RXD	GPIO_TRIG1	KEY_ROW2	SM_URTI_RXD		KEY_COL1			GPIO25
GPIO26	URT5_TXD	RGMII_PTP_PPS_O		SM_URTI_TXD	USB2_DRV_VBUS			cpu_rst_bypass_PDBoot	GPIO26
GPIO27	TW3_SCL	URT4_TXD		SM_URTI_RTSn					GPIO27
GPIO28	TW3_SDA	URT4_RXD		SM_URTI_CTSn					GPIO28
GPIO29		URT4_DE	KEY_ROW4	SM_URTI_RXD		KEY_COL4	SPI4_SDI		GPIO29
GPIO30		URT4_REn	KEY_ROW5	SM_URTI_TXD		KEY_COL5	SPI4_SCLK		GPIO30
GPIO31		RGMII_MDC			SPI5_SS3n	SPI3_SS2n	SPI4_SS2n		GPIO31
GPIO32		RGMII_MDIO				SPI3_SS3n	SPI4_SS3n		GPIO32
GPIO33	RGMII1_TD0	RMI11_TXD0			SM_CAN0_TX	SPI3_SS1n	SPI4_SS1n	software_strap[2]_PDBoot	GPIO33
GPIO34	RGMII1_TD1	RMI11_TXD1			SM_CAN0_RX				GPIO34
GPIO35	RGMII1_TD2	RMI12_TXD0	KEY_COL7	URT5_RXD			SPI4_SS0n		GPIO35
GPIO36	RGMII1_TD3	RMI12_TXD1		URT5_TXD			SPI4_SDO	software_strap[3]_PDBoot	GPIO36
GPIO37	RGMII1_RD0	RMI11_RXD0			SM_CAN1_TX		SPI5_SDI		GPIO37
GPIO38	RGMII1_RD1	RMI11_RXD1			SM_CAN1_RX		SPI5_SDO		GPIO38
GPIO39	RGMII1_RD2	RMI12_RXD0	KEY_ROW6	URT6_RXD		SPI4_SS3n			GPIO39
GPIO40	RGMII1_RD3	RMI12_RXD1	KEY_ROW7	URT6_TXD		SPI5_SS2n	SPI4_SS2n		GPIO40
GPIO41	RGMII1_RXC	RMI11_CRS0V					SPI5_SCLK		GPIO41
GPIO42	RGMII1_TXC	RMI12_CRS0V	KEY_ROW8	URT7_RXD					GPIO42
GPIO43	RGMII1_TXCTL	RMI11_TXEN				SPI4_SCLK			GPIO43
GPIO44	RGMII1_RXCTL	RMI12_TXEN	KEY_ROW9	URT7_TXD		SPI4_SS0n	SPI4_SDI	software_strap[0]_PDBoot	GPIO44
GPIO45	RGMII1_CLKOUT	RMI11_REFCLK							GPIO45
GPIO46	SDIO1_Cdn	SDIO2_Cdn	KEY_COL0		SM_URTI_RSTn	KEY_ROW9	DSI_TE		GPIO46
GPIO47	SDIO1_WP	SDIO2_WP	KEY_COL1	RMI12_REFCLK	SM_URTI_CTS	KEY_ROW8			GPIO47
GPIO48	RGMII2_TD0				SPI5_SS0n	SPI4_SS2n	SPI3_SS3n		GPIO48
GPIO49	RGMII2_TD1				SPI5_SDO	SPI4_SS3n	SPI3_SS2n		GPIO49
GPIO50	RGMII2_TD2				SPI5_SCLK		SPI3_SS1n		GPIO50
GPIO51	RGMII2_TD3						SPI3_SS0n		GPIO51
GPIO52	RGMII2_RD0					SPI4_SS2n	SPI3_SDO		GPIO52
GPIO53	RGMII2_RD1					SPI4_SS3n	SPI3_SCLK		GPIO53
GPIO54	RGMII2_RD2						SPI3_SDI		GPIO54
GPIO55	RGMII2_RD3				SPI5_SDI		SPI4_SS1n		GPIO55
GPIO56	RGMII2_RXC						SPI4_SS0n		GPIO56
GPIO57	RGMII2_TXC						SPI4_SDO		GPIO57
GPIO58	RGMII2_TXCTL						SPI4_SCLK		GPIO58
GPIO59	RGMII2_RXCTL						SPI4_SDI		GPIO59

SL2610 - 12x13

AA31	SoC.I2S1_LRCK	>>>SoC.I2S1_LRCK [14,15]
AA29	SoC.I2S1_BCLK	>>>SoC.I2S1_BCLK [14,15]
AA30	SoC.I2S1_DO	>>>SoC.I2S1_DO [14,15]
W29	SoC.I2S1_MCLK	>>>SoC.I2S1_MCLK [14]
AB30	SoC.GPIO4	>>>SoC.GPIO4 [21]
AC31	SoC.I2S2_LRCK	>>>SoC.I2S2_LRCK [21]
AC30	SoC.I2S2_BCLK	>>>SoC.I2S2_BCLK [21]
AA26	SoC.I2S2_DO	>>>SoC.I2S2_DO [21]
AA25	SoC.I2S2_DI	>>>SoC.I2S2_DI [21]
AB28	SoC.PDM_DI1	>>>SoC.PDM_DI1 [21]
AE30	SoC.GPIO10	>>>SoC.GPIO10 [14]
AD30	SoC.GPIO11_SM_PDM_CLKIO	>>>SoC.GPIO11_SM_PDM_CLKIO [21]
AE24	SoC.I2S3_LRCK	>>>SoC.I2S3_LRCK [21]
AC27	SoC.I2S3_BCLK	>>>SoC.I2S3_BCLK [21]
AF30	SoC.I2S3_DO	>>>SoC.I2S3_DO [21]
AC25	SoC.I2S3_DI	>>>SoC.I2S3_DI [21]
AG30	SoC.SPI2_SS0n&SDIO2_DAT3	>>>SoC.SPI2_SS0n&SDIO2_DAT3 [17]
AG28	SoC.SPI2_SS1n&SDIO2_DAT2	>>>SoC.SPI2_SS1n&SDIO2_DAT2 [17]
AG29	SoC.SPI2_SS2n&SDIO2_DAT1	>>>SoC.SPI2_SS2n&SDIO2_DAT1 [17]
AF31	SoC.SPI2_SS3n&SDIO2_DAT0	>>>SoC.SPI2_SS3n&SDIO2_DAT0 [17]
AH28	SoC.SPI2_SDO&SDIO2_CMD	>>>SoC.SPI2_SDO&SDIO2_CMD [17]
AF27	SoC.SPI2_SCLK&SDIO2_CLK&&STRP[SS1]@PDBoot	>>>SoC.SPI2_SCLK&SDIO2_CLK&&STRP[SS1]@PDBoot [10,17]
AF28	SoC.SPI2_SDI&SDIO2_Cdn	>>>SoC.SPI2_SDI&SDIO2_Cdn [17]
B4	SoC.TW2_SCL	>>>SoC.TW2_SCL [14,21]
B3	SoC.TW2_SDA	>>>SoC.TW2_SDA [14,21]
C6	SoC.GPIO25	>>>SoC.GPIO25 [14]
C5	SoC.GPIO26&&STRP[cpuRstByps]@PDBoot	>>>SoC.GPIO26&&STRP[cpuRstByps]@PDBoot [10,15]
A3	SoC.URT4_TXD	>>>SoC.URT4_TXD [21]
B2	SoC.URT4_RXD	>>>SoC.URT4_RXD [21]
A6	SoC.GPIO29	>>>SoC.GPIO29 [21]
B6	SoC.GPIO30	>>>SoC.GPIO30 [21]
C7	SoC.RGMII_MDC	>>>SoC.RGMII_MDC [13,16]
B7	SoC.RGMII_MDIO	>>>SoC.RGMII_MDIO [13,16]
C8	SoC.RGMII1_TD0&&STRP[SS2]@PDBoot	>>>SoC.RGMII1_TD0&&STRP[SS2]@PDBoot [10,16]
F10	SoC.RGMII1_TD1	>>>SoC.RGMII1_TD1 [16]
C9	SoC.RGMII1_TD2	>>>SoC.RGMII1_TD2 [16]
B9	SoC.RGMII1_TD3&&STRP[SS3]@PDBoot	>>>SoC.RGMII1_TD3&&STRP[SS3]@PDBoot [10,16]
B10	SoC.RGMII1_RD0	>>>SoC.RGMII1_RD0 [16]
F13	SoC.RGMII1_RD1	>>>SoC.RGMII1_RD1 [16]
D11	SoC.RGMII1_RD2	>>>SoC.RGMII1_RD2 [16]
A9	SoC.RGMII1_RD3	>>>SoC.RGMII1_RD3 [16]
B11	SoC.RGMII1_RXC	>>>SoC.RGMII1_RXC [16]
B12	SoC.RGMII1_TXC	>>>SoC.RGMII1_TXC [16]
B13	SoC.RGMII1_TXCTL&&STRP[SS0]@PUBoot	>>>SoC.RGMII1_TXCTL&&STRP[SS0]@PUBoot [10,16]
C13	SoC.RGMII1_RXCTL	>>>SoC.RGMII1_RXCTL [16]
A13	SoC.RGMII1_CLKOUT	>>>SoC.RGMII1_CLKOUT [16]
C14	SoC.GPIO46	>>>SoC.GPIO46 [21]
B14	SoC.RMI12_REFCLK	>>>SoC.RMI12_REFCLK [16]
F15	SoC.RGMII2_TXD0	>>>SoC.RGMII2_TXD0 [13]
F17	SoC.RGMII2_TXD1	>>>SoC.RGMII2_TXD1 [13]
C15	SoC.RGMII2_TXD2	>>>SoC.RGMII2_TXD2 [13]
D15	SoC.RGMII2_TXD3	>>>SoC.RGMII2_TXD3 [13]
B16	SoC.RGMII2_RXD0	>>>SoC.RGMII2_RXD0 [13]
A16	SoC.RGMII2_RXD1	>>>SoC.RGMII2_RXD1 [13]
C17	SoC.RGMII2_RXD2	>>>SoC.RGMII2_RXD2 [13]
C19	SoC.RGMII2_RXD3	>>>SoC.RGMII2_RXD3 [13]
B17	SoC.RGMII2_RXC	>>>SoC.RGMII2_RXC [13]
A18	SoC.RGMII2_TXC	>>>SoC.RGMII2_TXC [13]
B19	SoC.RGMII2_TXCTL	>>>SoC.RGMII2_TXCTL [13]
B18	SoC.RGMII2_RXCTL	>>>SoC.RGMII2_RXCTL [13]

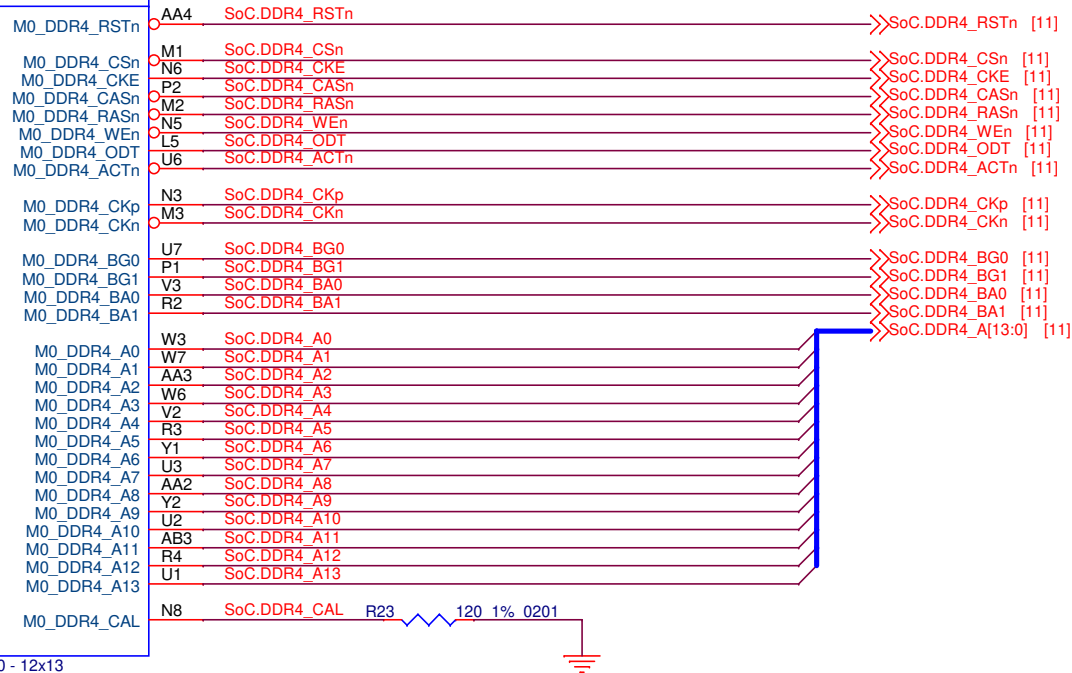
Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131

Title		
SL2610 CORE MODULE		
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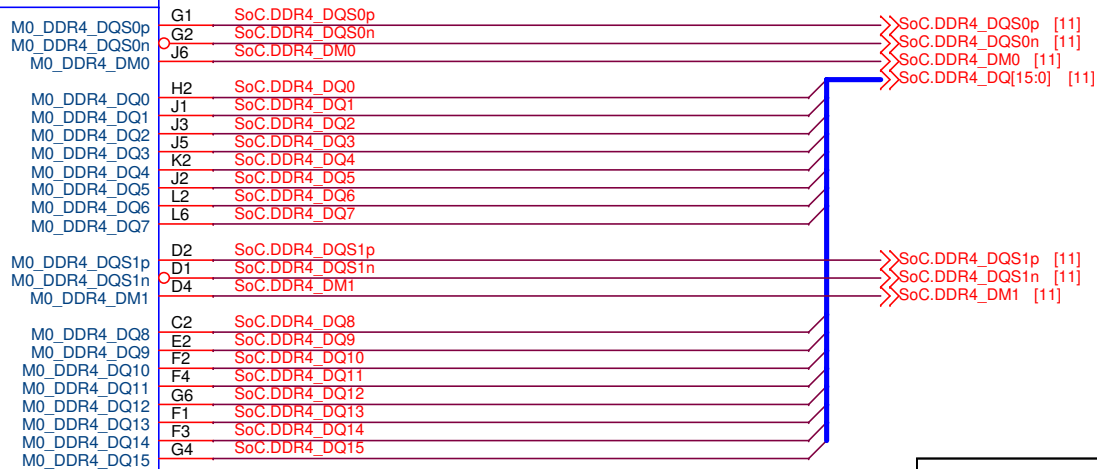
U1B

DDR4_SDRAM



U1C

DDR4_SDRAM



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06: SL1620 - DDR4_PHY

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U1G

MIPI - CSI

MIPI_CSI_CKp
MIPI_CSI_CKnMIPI_CSI_D0p
MIPI_CSI_D0n
MIPI_CSI_D1p
MIPI_CSI_D1n

MIPI_CSI_REXT

SL2610 - 12x13



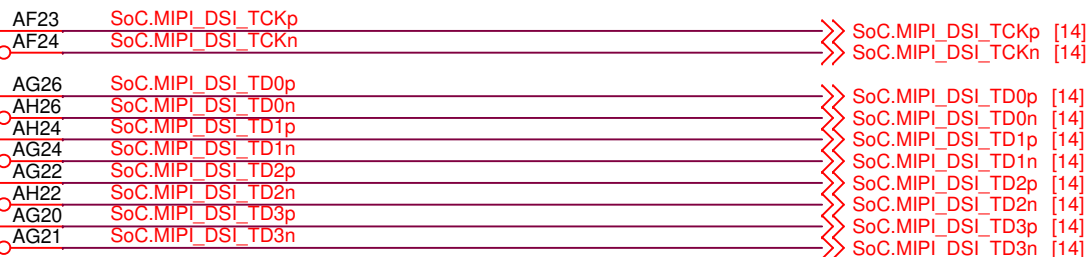
U1H

MIPI - DSI

MIPI_DSI_CKp
MIPI_DSI_CKnMIPI_DSI_D0p
MIPI_DSI_D0n
MIPI_DSI_D1p
MIPI_DSI_D1n
MIPI_DSI_D2p
MIPI_DSI_D2n
MIPI_DSI_D3p
MIPI_DSI_D3n

MIPI_DSI_REXT

SL2610 - 12x13



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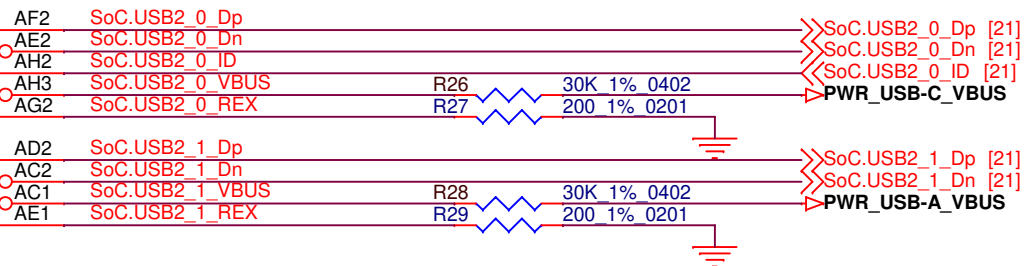
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U1F

USB2

USB2_0_Dp
USB2_0_Dn
USB2_0_ID
USB2_0_VBUS
USB2_0_REXT



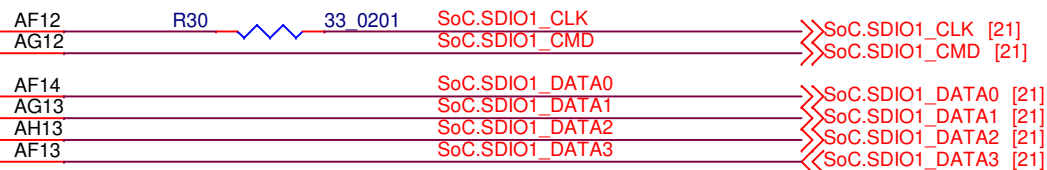
SL2610 - 12x13

U1J

SDIO1

SDIO1_CLK
SDIO1_CMD

SDIO1_DATA0
SDIO1_DATA1
SDIO1_DATA2
SDIO1_DATA3



SL2610 - 12x13

To M.2

U1I

EMMC

EMMC_RSTn
EMMC_CLK
EMMC_CMD
EMMC_STRB



SL2610 - 12x13

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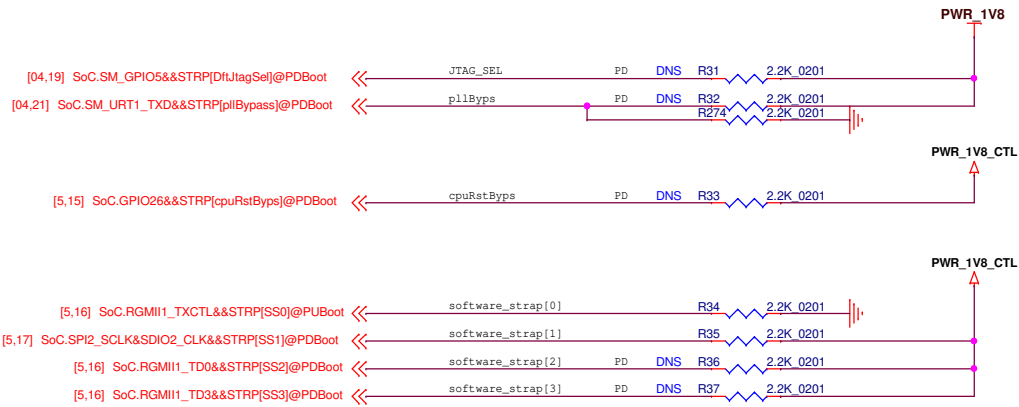
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JTAG_SEL 0: ATE/RMA Mode - but Functional JTAG is selected
1: ATE/RMA Mode - DFT JTAG is selected

p1lByps 0: No Bypass (Default)
1: All PLL bypassed

cpuRstByps 0: Enable reset logic inside cpu partition (Default)
1: Bypass reset logic inside cpu partition

software_strap[0]
1--> RevA; 0-->RevB and later version

software_strap[1]
1-->DDR4@2GB; 0-->DDR4@4GB

software_strap[2]
Default: 0

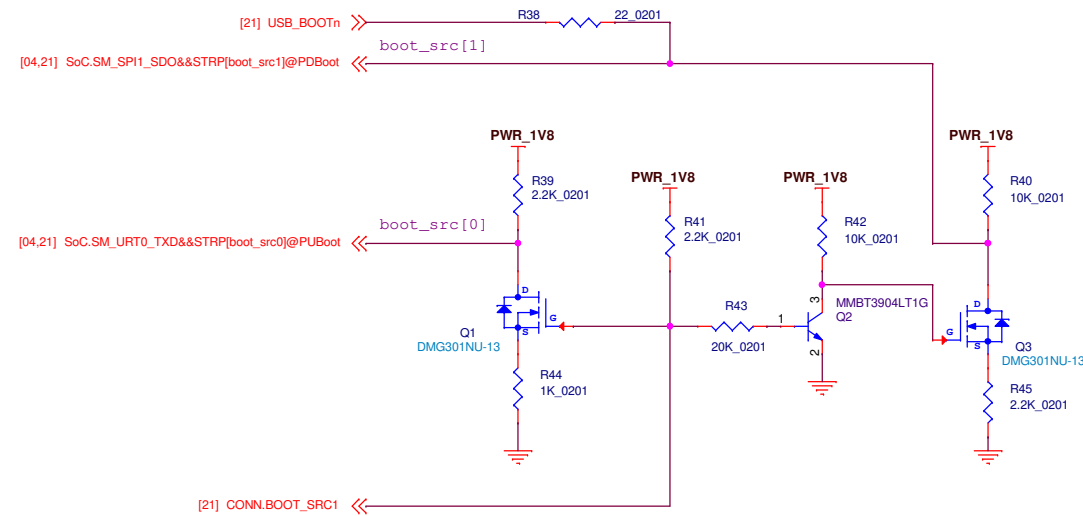
software_strap[3]
Default: 0

BOOT STRAP OPTION

BootSrc[1:0]	TYPE
2'b00	ROM boot from USB2
2'b01	ROM boot from xSPI_NOR
2'b10	ROM boot from EMMC default
2'b11	ROM boot from xSPI_NAND

Note for xSPI_NAND
1. CONN-VDDIO1P8.BOOT_SRC1 = Low (external SPI board header JP10 2-3 is ON)
2. HW rework Q3.G to GND

Note for SPI Clear_Boot
1. CONN-VDDIO1P8.BOOT_SRC1 = Low (external SPI board header JP10 2-3 is ON)
2. HW rework Q3.G to GND
3. HW rework R33=2.2K (cpuRstByp = 1)



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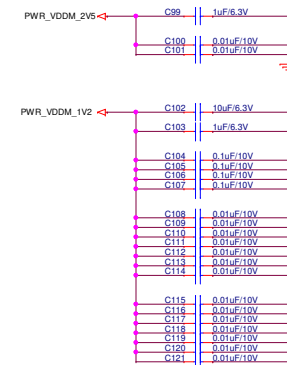


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10: SL2610 - STRAP		
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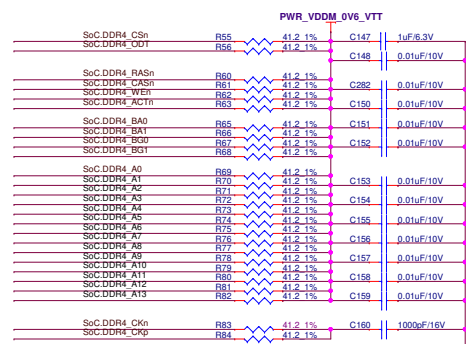
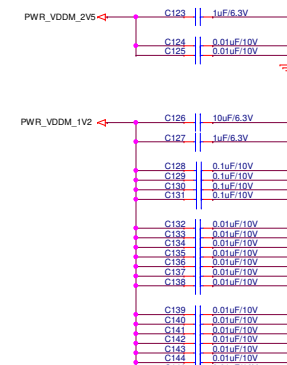
8Gb: IS43QR81024B-062AABL;
16Gb: MT40A2G8SA-062E;
& other qualified parts

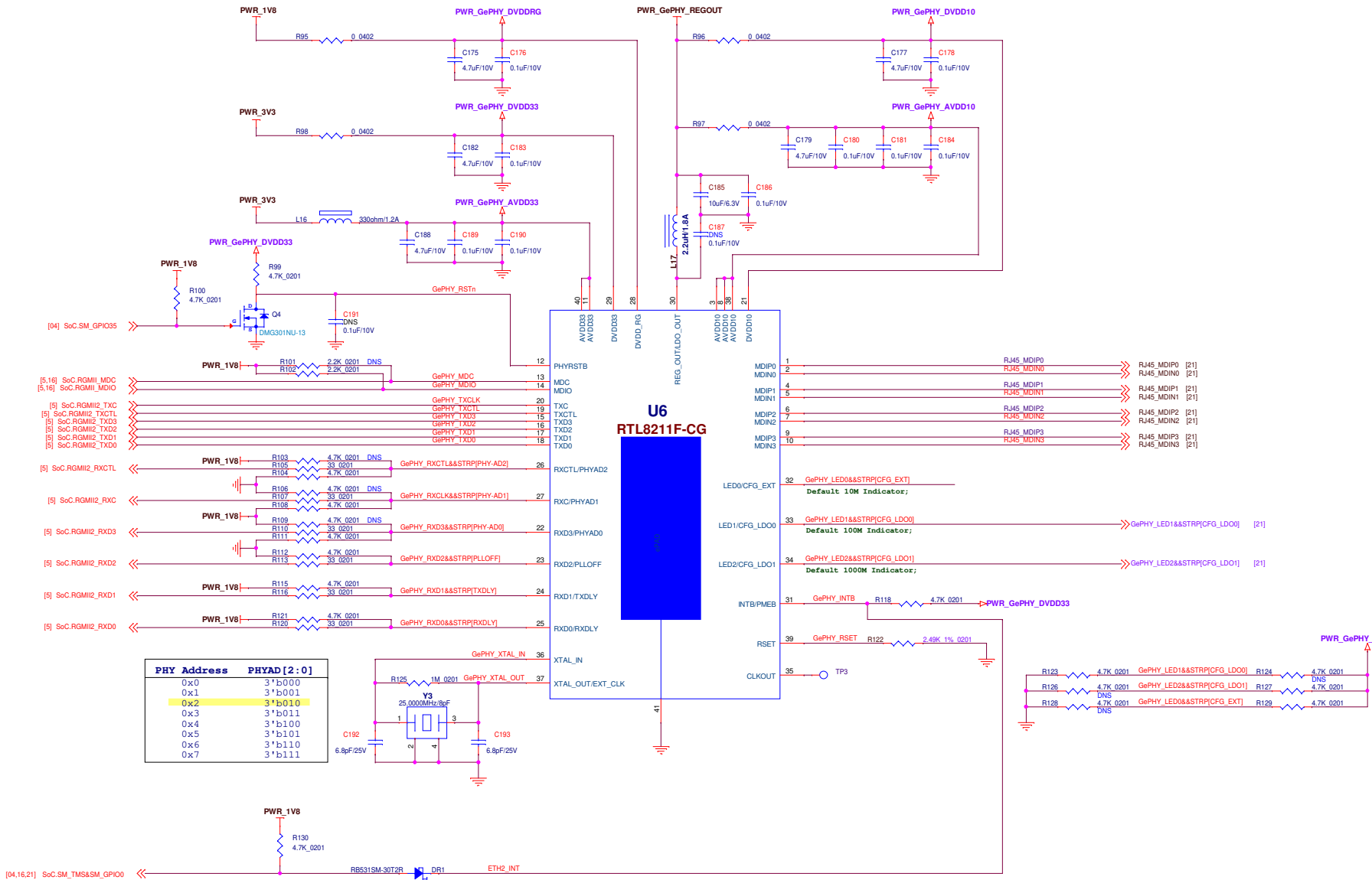
8Gb: IS43QR81024B-062AABL;
16Gb: MT40A2G8SA-062E;
& other qualified parts

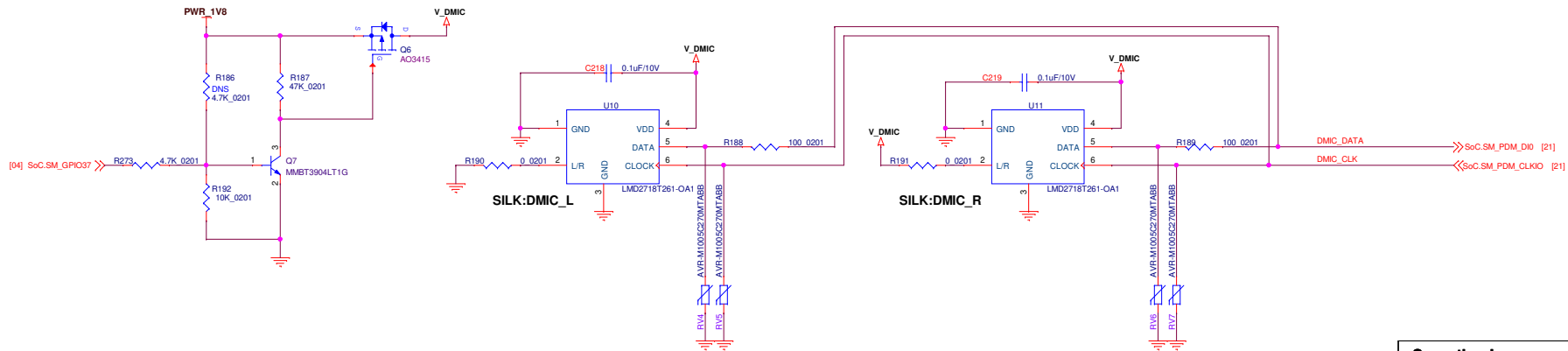
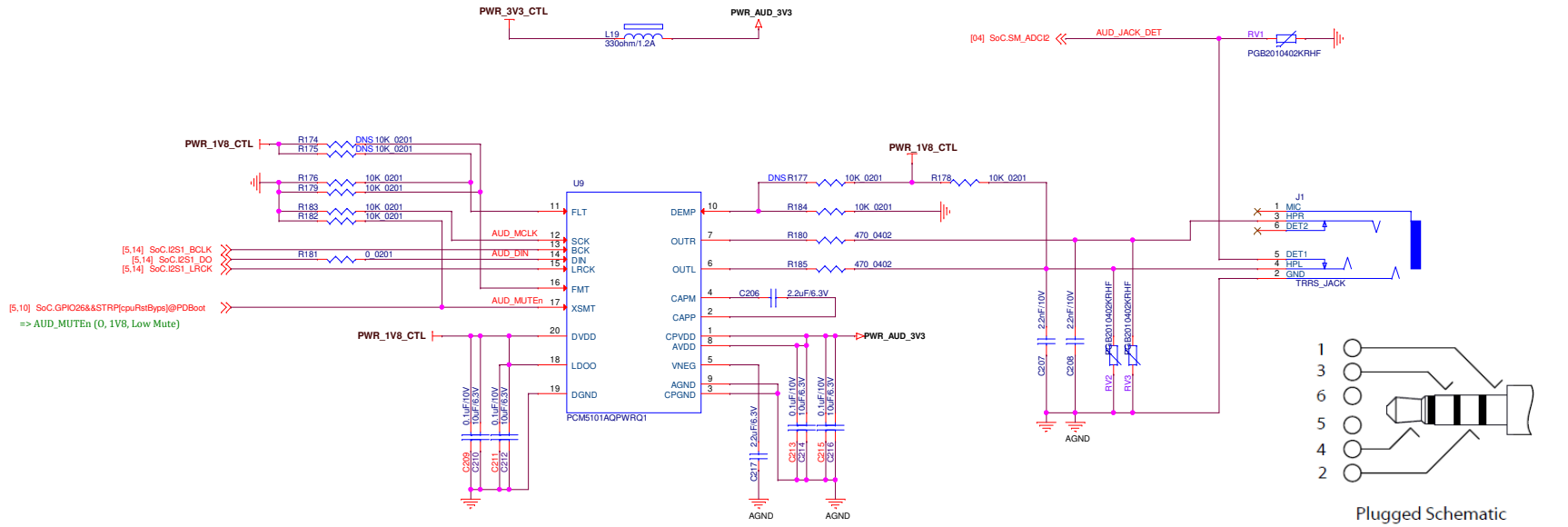
8Gb: IS43QR81024B-062AABL;
16Gb: MT40A2G8SA-062E;
& other qualified parts

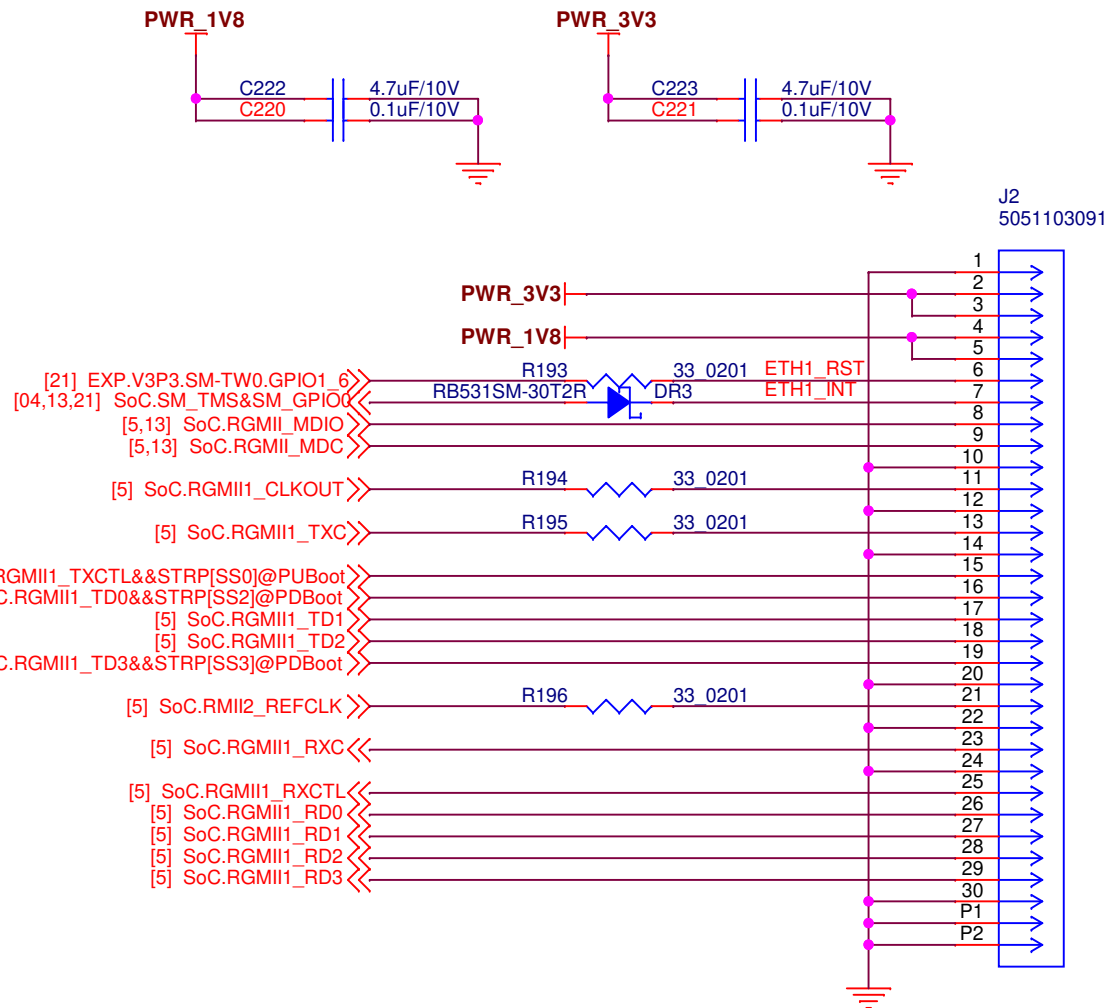


8Gb: IS43QR81024B-062AABL;
16Gb: MT40A2G8SA-062E;
& other qualified parts









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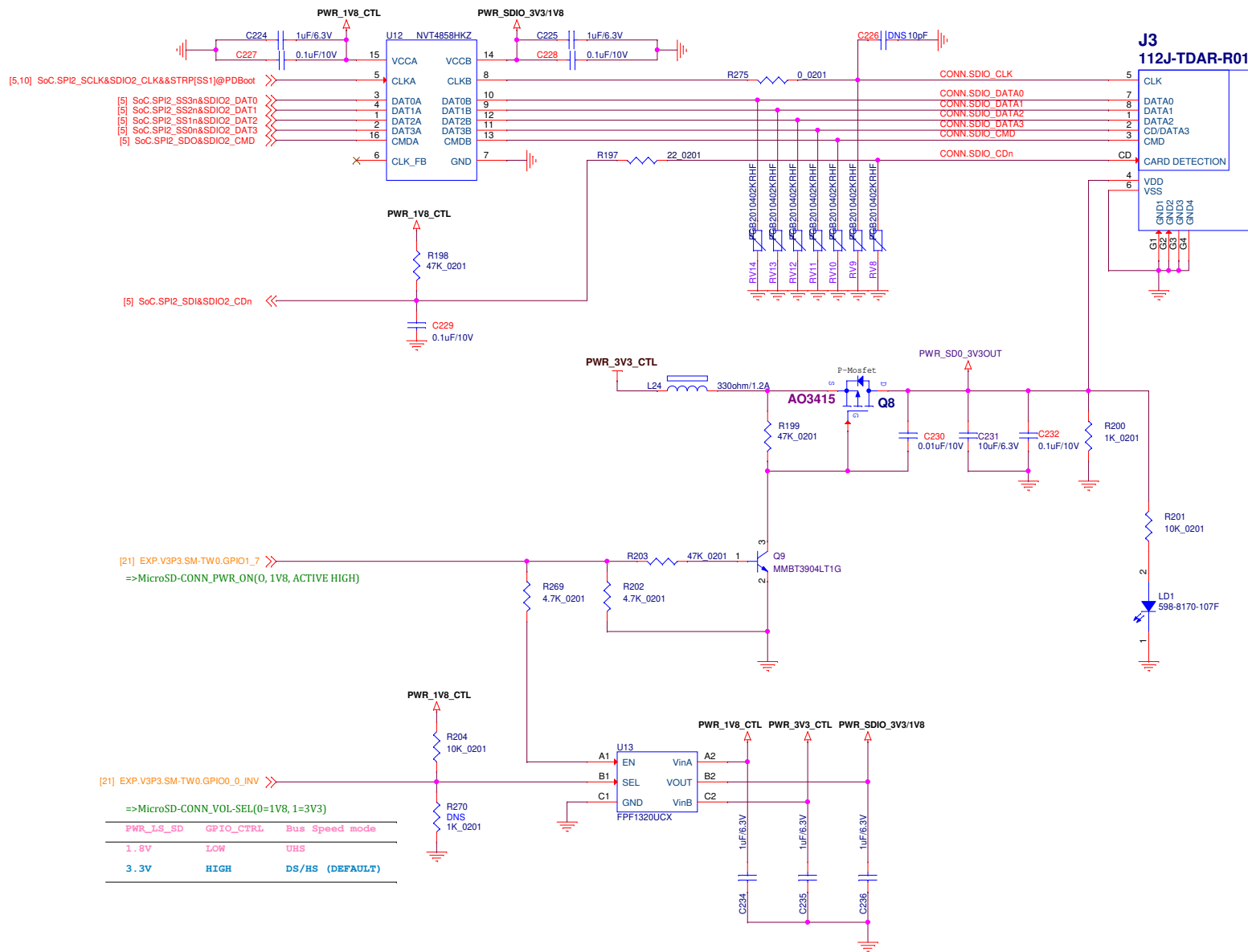
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Date:

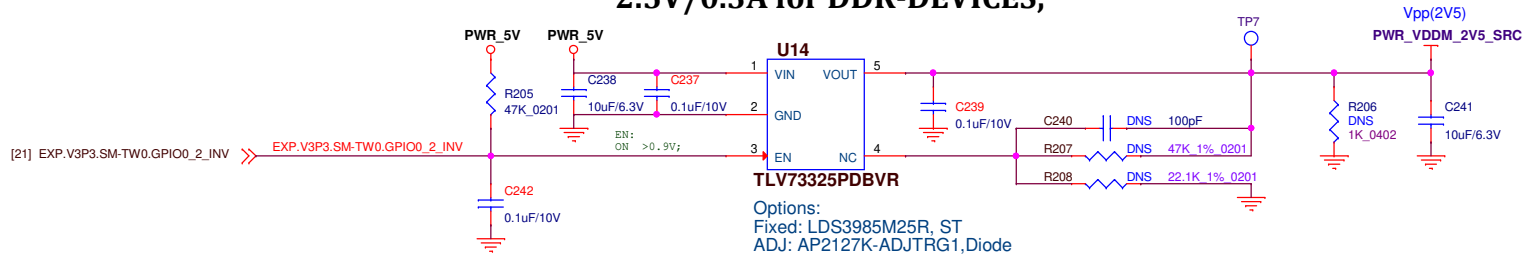
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2.5V/0.3A for DDR-DEVICES;



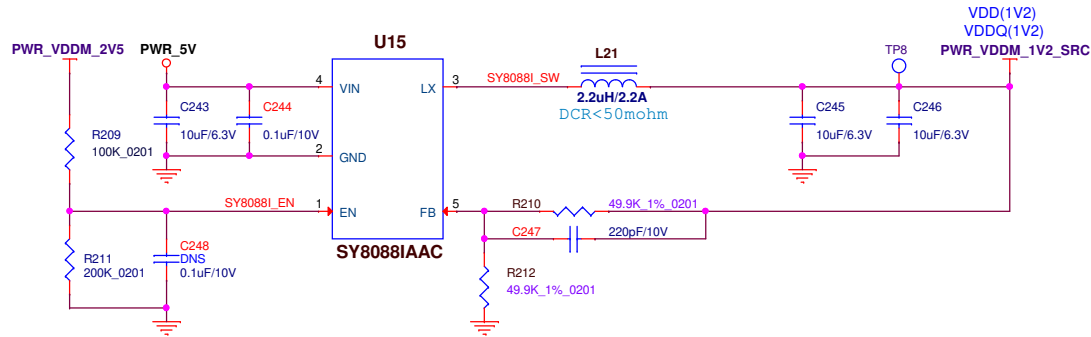
Vpp(2V5)

VDD(1V2)

VDDQ(1V2)

- 1)VPP must ramp at the same time or before VDD;
- 2)VDD must be greater than or equal to VDDQ. i.e., VPP>=VDD>=VDDQ on power-up sequence.

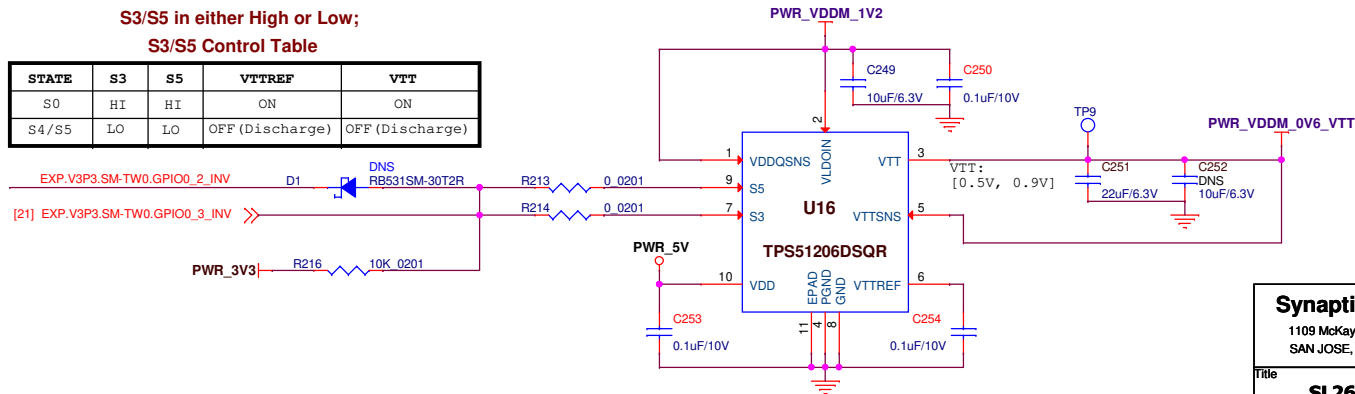
Power-Up Sequence For DDR4 DEVICE



VTT (0.6V) 1.2A Supply for DDR-DEVICES;

S3/S5 in either High or Low;
S3/S5 Control Table

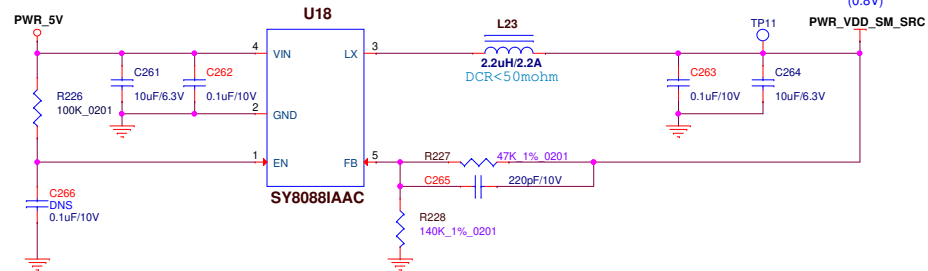
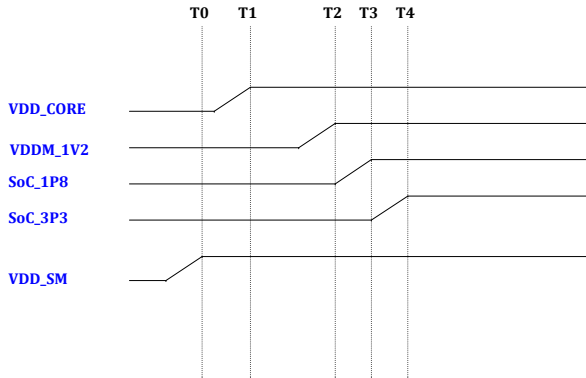
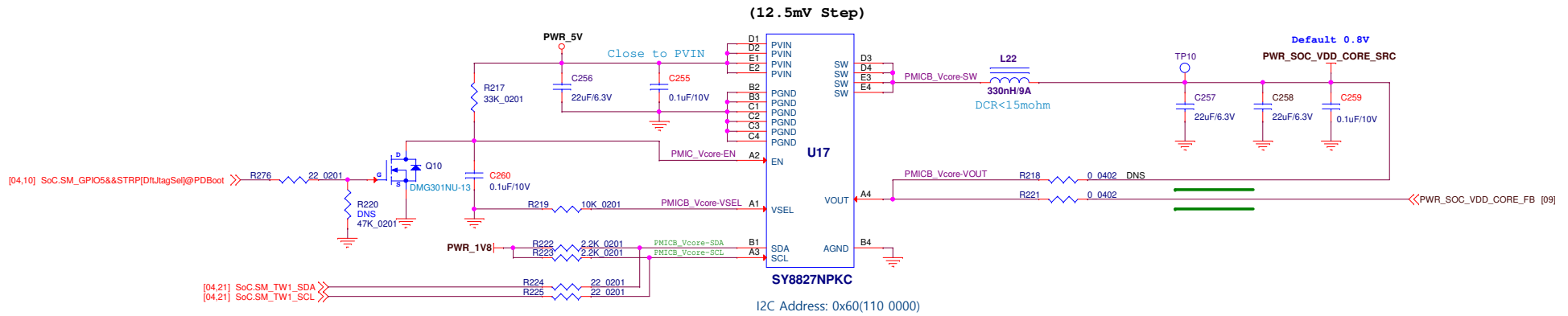
STATE	S3	S5	VTTREF	VTT
S0	HI	HI	ON	ON
S4/S5	LO	LO	OFF (Discharge)	OFF (Discharge)



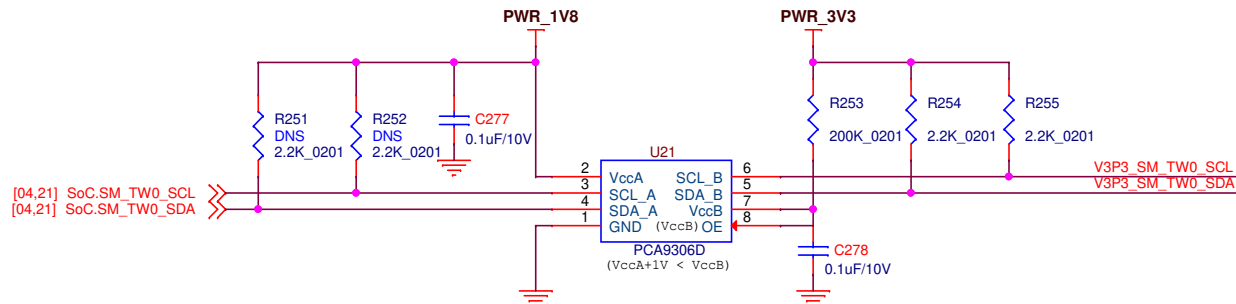
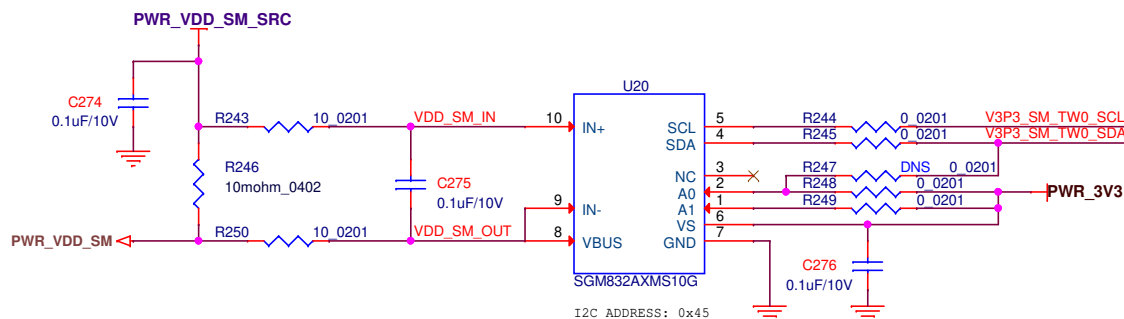
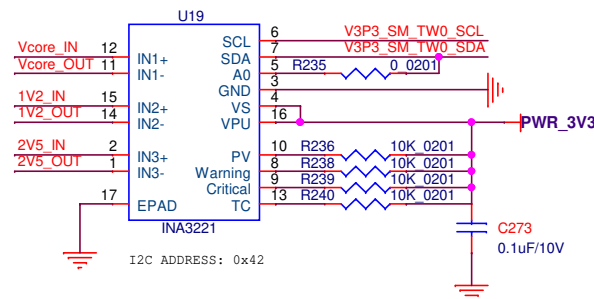
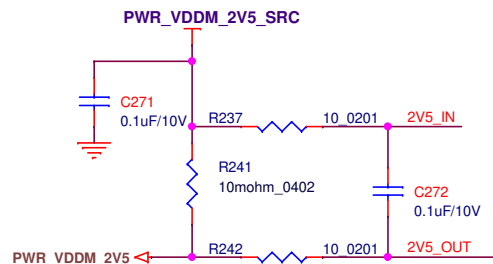
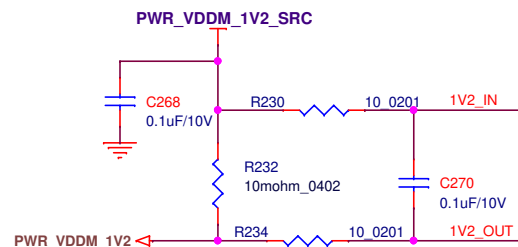
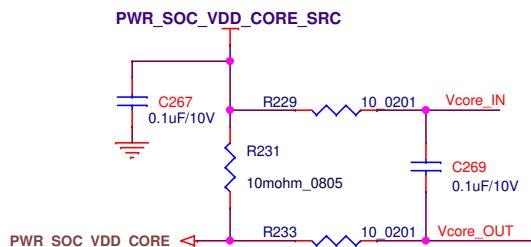
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0.8V/6A for SL2610 SOC_VDD_CORE



SL2610 Recommended Power Sequence



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